HN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,184	10/30/2001	Frederic Reblewski	109894-129746	4114

22907 7590 03/10/2005

BANNER & WITCOFF
1001 G STREET N W
SUITE 1100
WASHINGTON, DC 20001

EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,184	REBLEWSKI, FREDERIC	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/21/02, 3/14/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *(PTO-1449) 8/11/03*.

DETAILED ACTION

1. Claims 1-34 of the application have been examined.

Drawings

2. The drawings submitted on October 30, 2001 are accepted.

Specification

3. The disclosure is objected to because of the following informalities:

Specification Page 1, Line 25 to Page 2, Line1, "test stimuli are either generated on the workstation ... and then transfer to various logic boards for input into emulation ICs" appears to be incorrect and it appears that it should be "test stimuli are either generated on the workstation ... and then transferred to various logic boards for input into emulation LEs".

Specification Page 7, Lines 7-8, "co-pending U.S. Patent application number <insert the CIP number here>, to be described" is incorrect. The applicant is required to provide the correct application number here.

Specification Page 10, Line 7, "includingre-creation" appears to be incorrect and it appears that it should be "including re-creation".

Specification Page 12, Line 1, "Control module 602 is equipped" appears to be incorrect and it appears that it should be "Control module 402 is equipped".

Specification Page 13, Line 17, "to locally pre-processes" appears to be incorrect and it appears that it should be "to locally pre-process".

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5.1 Claim 1 states in part, "locally retrieve from said emulation ICs state data of emulation state circuit elements". How is "emulation state circuit elements" different from "emulation circuit elements" used in claim 11?

5.2 Claim 2 states in part, "local retrieval of state data of the emulation state circuit elements". How is "emulation state circuit elements" different from "emulation circuit elements" used in claim 11?

5.3 Claim 4 states in part, "locally apply said locally generated testing stimuli to the partition of the IC design being emulated". The partition of the IC design being emulated is in the form of netlist. One cannot locally apply said locally generated testing stimuli to the partition of the IC design being emulated. One can apply the test stimuli only to a circuit.

5.4 Claim 7 states in part, "locally retrieving from emulation ICs of said logic board state data of emulation state circuit elements of a partition of an IC design being emulated". How is "emulation state circuit elements" different from "emulation circuit elements" used in claim 11?

5.5 Claim 9 states in part, "applying said locally generated testing stimuli to the partition of the IC design being emulated". The partition of the IC design being emulated is in the form of netlist. One cannot locally apply said locally generated testing stimuli to the partition of the IC design being emulated. One can apply the test stimuli only to a circuit.

5.6 Claim 11 states in part, "apply said locally generated testing stimuli to emulation circuit elements of said partition of the IC design being emulated". The partition of the IC design being emulated is in the form of a netlist. What is meant by emulation circuit elements of said partition of the IC design being emulated? The partition of the IC design being emulated does not have emulation circuit elements.

5.7 Claim 14 states in part, "locally applying said locally generated testing stimuli to emulation circuit elements of a partition of an IC design being emulated". The partition of the IC design being emulated is in the form of a netlist. What is meant by emulation circuit elements of a partition of an IC design being emulated? The partition of an IC design being emulated does not have emulation circuit elements.

5.8 Claim 16 states in part, "retrieving state data of emulation state circuit elements from the emulation ICs, responsive monitor and report requests received through input/output (I/O) pins of the logic boards, and retrieving state data of the emulation state circuit elements from the emulation ICs". How is "emulation state circuit elements" different from "emulation circuit elements" used in claim 11?

5.9 Claim 19 states in part, "apply the generated stimuli to the emulated circuit elements of the partitions of the IC design being emulated". The emulated circuit elements of the partition of the IC design being emulated are in the form of netlist. One cannot locally apply the generated stimuli to the emulated circuit elements of the

partition of the IC design being emulated. One can apply the test stimuli only to a circuit.

5.10 Claim 22 states in part, "locally and correspondingly retrieving state data of emulation state circuit elements of partitions of an IC design to be monitored from the emulation ICs". How is "emulation state circuit elements" different from "emulation circuit elements" used in claim 11?

5.11 Claim 24 states in part, "locally and corresponding applying the generated testing stimuli to selected ones of the emulation circuit elements of partitions of an IC design being emulated". The partition of the IC design being emulated is in the form of a netlist. What is meant by emulation circuit elements of said partition of the IC design being emulated? The partition of the IC design being emulated does not have emulation circuit elements.

5.12 Claim 26 states in part, "locally retrieve state data of emulation state circuit elements of a partition of an IC design being emulated to monitor, analyze the retrieved state data of the emulation state circuit elements". How is "emulation state circuit elements" different from "emulation circuit elements" used in claim 11?

5.13 Claim 28 states in part, "locally apply the generated testing stimuli to the partition of the IC design being emulated". The partition of the IC design being emulated is in the

form of netlist. One cannot locally apply the generated stimuli to the partition of the IC design being emulated. One can apply the test stimuli only to a circuit.

5.14 Claim 30 states in part, "locally retrieving on said emulation IC, using on-chip data processing resources, emulation state circuit elements of a partition of an IC design being emulated;

locally analyzing state data of the emulation state circuit elements".

What is meant by retrieving emulation state circuit elements? The circuit elements are hardware elements. How does one retrieve the hardware elements during emulation? How is "emulation state circuit elements" different from "emulation circuit elements" used in claim 11?

5.15 Claim 32 states in part, "locally apply the generated testing stimuli to a partition of an IC design being emulated". The partition of an IC design being emulated is in the form of netlist. One cannot locally apply the generated testing stimuli to a partition of an IC design being emulated. One can apply the test stimuli only to a circuit.

5.16 Claim 34 states in part, "locally applying the testing stimuli, using said on-chip data processing resources, to emulation circuit elements of a partition of an IC design". The partition of the IC design being emulated is in the form of a netlist. What is meant by emulation circuit elements of a partition of an IC design? The partition of an IC design does not have emulation circuit elements.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-34 are rejected under 35 U.S.C. 102(b) as being anticipated by **Quayle et al.** (U.S. Patent 6,694,464).

7.1 **Quayle et al.** teaches method and apparatus for dynamically testing electrical interconnect. Specifically, as per claim 1, **Quayle et al.** teaches a logic board designed for circuit emulation (Abstract, L1 and L3-9; Fig. 11; CL1, L24-26; CL7, L12-13; CL16, L51-54), comprising

a plurality of input/output (I/O) pins (Abstract, L8-9; CL4, L27-30; CL16, L62-64);

a plurality of emulation integrated circuits (IC), each having reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of a partition of an IC design (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13); and

a plurality of on-board data processing resources coupled to the emulation ICs (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26) to locally retrieve from the emulation ICs state data of emulation state circuit elements (CL18, L5-9; CL23, L63-65), responsive to a monitor and report request received through the I/O pins (CL5, L2-4; Fig.20a,

Item 238), and to locally analyze the retrieved state data to detect occurrence of one or more events, as well as report on the occurrence of the one or more events upon their detection through the I/O pins (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Per claim 2: **Quayle et al.** teaches that the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the responsive local retrieval of state data of the emulation state circuit elements (CL18, L5-9; CL23, L63-65), local analysis of the retrieved state data, and reporting of event detection (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59), and a processor coupled to the storage medium to execute the programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206).

Per claim 3: **Quayle et al.** teaches that at least one of the emulation ICs comprises on-chip data processing resources (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18), to cooperate and assist the on-board data processing resources to perform the local monitoring and reporting of monitored events (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Per claim 4: **Quayle et al.** teaches that the on-board data processing resources are further employed to locally generate a plurality of testing stimuli, and locally apply the locally generated

testing stimuli to the partition of the IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), responsive to a testing request received through the I/O pins (Fig. 19, BP clocks).

Per claim 5: **Quayle et al.** teaches that the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the responsive local generation and application of stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), and a processor coupled to the storage medium to execute the programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206).

Per claim 6: **Quayle et al.** teaches that at least one of the emulation ICs comprises on-chip data processing resources (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18), to cooperate and assist the on-board data processing resources to perform the local generation and application of testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

7.2 As per claim 7, **Quayle et al.** teaches in an emulation apparatus, a method of operation (Abstract, L1 and L3-9; Fig. 11; CL1, L24-26; CL7, L12-13; CL16, L51-54), comprising:

receiving by an emulation logic board, through input/output (I/O) pins of the logic board, a monitor and report request (CL5, L2-4; Fig.20a, Item 238);

in response, locally retrieving from emulation ICs of the logic board state data of emulation state circuit elements of a partition of an IC design being emulated (CL18, L5-9; CL23, L63-65);

locally analyzing the retrieved state data to detect occurrence of one or more events (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59); and

reporting through the I/O pin, of the logic board occurrence of the one or more events, upon detection of their occurrence (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Per claim 8: **Quayle et al.** teaches that at least some of the analysis and detection are performed by on-chip data processing resources of the emulation ICs, in lieu of retrieving the state data from the emulation ICs (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18), and then analyzing the state data to detect for the one or mare events (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Per claim 9: **Quayle et al.** teaches that the method further comprises locally generating on the logic board a plurality of testing stimuli, and applying the locally generated testing stimuli to the partition of the IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), responsive to an external testing request received by the logic board through the I/O pins of the logic board (Fig. 19, BP clocks).

Per claim 10: **Quayle et al.** teaches that at least some of the generation of testing stimuli are performed (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), by on-chip data processing resources of the emulation ICs instead (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18).

7.3 As per claim 11, **Quayle et al.** teaches a logic board designed for circuit emulation (Abstract, L1 and L3-9; Fig. 11; CL1, L24-26; CL7, L12-13; CL16, L51-54), comprising

a plurality of input/output (I/O) pins (Abstract, L8-9; CL4, L27-30; CL16, L62-64);

a plurality of emulation integrated circuits (IC), each having reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of a partition of an IC design (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13); and

a plurality of on-board data processing resources coupled to the emulation ICs to locally generate a plurality of testing stimuli, and locally apply the locally generated testing stimuli to emulation circuit elements of the partition of the IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), responsive to a testing request received through the I/O pins (Fig. 19, BP clocks).

Per claim 12: **Quayle et al.** teaches that the on-board data processing resources comprise a storage medium having stored therein programming instructions designed to operate the logic board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the responsive local generation and application of stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), and a processor coupled to the storage medium to

execute the programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206).

Per claim 13: **Quayle et al.** teaches that at least one of the emulation ICs comprises on-chip data processing resources (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18), to cooperate and assist the on-board data processing resources to perform the local generation and application of testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

7.4 As per claim 14, **Quayle et al.** teaches in an emulation apparatus, a method of operation (Abstract, L1 and L3-9; Fig. 11; CL1, L24-26; CL7, L12-13; CL16, L51-54), comprising:

receiving by a logic board, through input/output (I/O) pins of the logic board, a testing request (Fig. 19, BP clocks);

in response, locally generating on the logic board a plurality testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65); and

locally applying the locally generated testing stimuli to emulation circuit elements of a partition of an IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

Per claim 15: **Quayle et al.** teaches that at least some of the generation of testing stimuli are performed (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), by on-chip data processing resources of the emulation ICs instead (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18).

7.5 As per claim 16, **Quayle et al.** teaches an emulation system (Fig. 12; CL18, L26-31), comprising:

a plurality of logic boards (Fig. 12; CL18, L26-31), each having a plurality of emulation integrated circuits (IC) including reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of partitions of an IC design (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13), and on-board data processing resources to locally and correspondingly retrieving state data of emulation state circuit elements from the emulation ICs (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26), responsive monitor and report requests received through input/output (I/O) pins of the logic boards (CL5, L2-4; Fig.20a, Item 238), and retrieving state data of the emulation state circuit elements from the emulation ICs, locally and correspondingly analyzing the retrieved state data for one or more events, and reporting occurrence of the one or more events through the I/O pins upon their detection (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59); and

a workstation coupled to the logic board electronic design automation (EDA) software(CL23, L29-31; C26, L10-13; Fig. 20, Item 700), to provide the logic boards with the monitor and report requests (CL5, L2-4; Fig.20a, Item 238).

Per claim 17: **Quayle et al.** teaches that the on-board data processing resources of each of the Emulation IC comprise storage medium having stored therein programming instructions to operate the logic board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the local and corresponding retrieval, analysis, and reporting (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Per claim 18: **Quayle et al.** teaches that at least one of the emulation ICs of the logic boards comprises on-chip data processing resources (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18), to cooperate and assist the on-board data processing resources to perform the local and corresponding retrieval, analysis, and reporting (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

7.6 As per claim 19, **Quayle et al.** teaches an emulation system (Fig. 12; CL18, L26-31), comprising:

a plurality of logic boards (Fig. 12; CL18, L26-31), each having a plurality of emulation integrated circuits (IC) including reconfigurable logic and interconnect resources reconfigurable to emulate circuit elements of partitions of an IC design (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13), and on-board data processing resources to locally and correspondingly generate testing stimuli, and apply the generated stimuli to the emulated circuit elements of the partitions of the IC design being emulated(CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), responsive to testing requests received through input/output (I/O) pins of the logic boards (Fig. 19, BP clocks); and

a workstation coupled to the logic board, including electronic design automation (EDA) software (CL23, L29-31; C26, L10-13; Fig. 20, Item 700), to provide the logic boards with the testing requests (Fig. 19, BP clocks).

Per claim 20: **Quayle et al.** teaches that the on-board data processing resources of each of the logic board comprise storage medium having stored therein programming instructions designed to operate the logic board (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), to perform the local and corresponding generation and application of testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

Per claim 21: **Quayle et al.** teaches that at least one of the emulation ICs comprises on-chip data processing resources (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18), to cooperate and assist the on-board data processing resources of the logic board to perform the local and corresponding generation and application of testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

7.7 As per claim 22, **Quayle et al.** teaches in an emulation system, a method of operation (Fig. 12; CL18, L26-31), comprising:

locally and correspondingly retrieving state data of emulation state circuit elements of partitions of an IC design to be monitored from the emulation ICs (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26), the partitions of the IC design being emulated by reconfigurable logic and interconnect resources of emulation ICs of logic boards of the emulation system (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13);

locally and correspondingly analyzing the retrieved state data to detect one or more event; and reporting the detected ones of the one or more events upon their detection (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Per claim 23: **Quayle et al.** teaches that at least some of the performances of local and corresponding retrieval, analysis, and reporting are assisted (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59), by on-chip data processing resources of the emulation ICs of the logic boards (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18).

7.8 As per claim 24, **Quayle et al.** teaches in an emulation system, a method of operation (Fig. 12; CL18, L26-31), comprising:

locally and correspondingly generating testing stimuli; and locally and corresponding applying the generated testing stimuli to selected ones of the emulation circuit elements of partitions of an IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

Per claim 25: **Quayle et al.** teaches that at least some of the performances of local and corresponding generation and application of testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), are assisted by on-chip data processing resources of the emulation lCs of the logic boards (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18).

7.9 As per claim 26, **Quayle et al.** teaches an emulation integrated circuit (IC) (CL1, L24-33), comprising

a plurality of reconfigurable logic and interconnect resources (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13); and

on-chip data processing resources coupled to the reconfigurable logic and interconnect resources (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18) to locally retrieve state data of emulation state circuit elements of a partition of an IC design being emulated (CL18, L5-9; CL23, L63-65), to monitor, analyze the retrieved state data of the emulation state circuit elements to detect occurrence of one or more events, and report on occurrence of the one or more events upon detecting their occurrence (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Per claim 27: **Quayle et al.** teaches that the on-chip data processing resources comprises storage medium having stored therein programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), designed to perform the local analysis and reporting (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Per claim 28: **Quayle et al.** teaches that the on-chip data processing resources further locally generate testing stimuli, and locally apply the generated testing stimuli to the partition of the IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

Per claim 29: **Quayle et al.** teaches that the on-chip data processing resources comprises storage medium having stored therein programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), designed to

perform the local generation and application of testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

7.10 As per claim 30, **Quayle et al.** teaches in an emulation integrated circuit (IC), a method of operation (CL1, L24-33), comprising

locally retrieving on the emulation IC, using on-chip data processing resources, emulation state circuit elements of a partition of an IC design being emulated (CL18, L5-9; CL23, L63-65);

locally analyzing state data of the emulation state circuit elements, using on chip data processing resources, to detect occurrence of one or more events; and reporting on occurrence of the one or more events upon detecting their occurrence (Fig. 20a, Item 240; CL18, L5-9; CL23, L60-62; CL23, L63-65; CL25, L54-59).

Per claim 31: **Quayle et al.** teaches that the method comprises locally and correspondingly generating testing stimuli; and locally and corresponding applying the generated testing stimuli to selected ones of the emulation circuit elements of partitions of an IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

7.11 As per claim 32, **Quayle et al.** teaches an emulation integrated circuit (IC) (CL1, L24-33), comprising

a plurality of reconfigurable logic and interconnect resources (Abstract, L3-9; CL1, L26-36; Fig. 11; CL7, L12-13); and

on-chip data processing resources coupled to the reconfigurable logic and interconnect resources (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18) to locally generate testing stimuli, locally apply the generated testing stimuli to a partition of an IC design being emulated (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

Per claim 33: **Quayle et al.** teaches that the on-chip data processing resources comprises storage medium having stored therein programming instructions (Fig. 11, Items 206 and 204; CL17, L2-3; CL17, L15-20; CL17, L24-26; Fig. 20, Items 224, 226 and 206), designed to perform the local generation and application of testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65).

7.12 As per claim 34, **Quayle et al.** teaches in an emulation integrated circuit (IC), a method of operation (CL1, L24-33), comprising:

locally generating on the emulation IC testing stimuli, using on-chip data processing resources; and locally applying the testing stimuli (CL22, L56-62; Fig. 19, Item 204; CL23, L60-65), using the on-chip data processing resources, to emulation circuit elements of a partition of an IC design (Fig. 20c, Item 236; CL7, L44-46; CL25, L54-59; CL26, L10-18).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
March 1, 2005

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER